



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/530,562	04/07/2005	Masahiko Hata	Q87267	8996
23373	7590	05/02/2007		
SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVENUE, N.W. SUITE 800 WASHINGTON, DC 20037			EXAMINER HITESHEW, FELISA CARLA	
			ART UNIT 1722	PAPER NUMBER
			MAIL DATE 05/02/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

**Application No.**

10/530,562

**Applicant(s)**

MASAHITO HATA

**Examiner**

Felisa C. Hiteshew

**Art Unit**

1722

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.138(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                       | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. ____                                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>04/07/2005 &amp; 01/24/2007</u> .                             | 6) <input type="checkbox"/> Other: ____                           |

Art Unit: 1722

***Priority***

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

***Information Disclosure Statement***

The PTOL 1449 filed on 04/07/2005 and 01/24/2007 have been received, reviewed and considered.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Japanese Abstract 63-199460 A (JP '460 A) in view of Japanese Abstract 63-52473 A (JP '473 A).

JP '460 A teaches a semiconductor apparatus comprising a silicon thin film (12) on a semiconductor substrate (11) made of n-type GaAs so that the conductivity type of the film is identical with the substrate, and by forming an ohmic electrode corresponding with the silicon thin film (12), and a ohmic electrode (13) can be formed corresponding with the silicon thin film (12). The n-type GaAs layer (112) has an impurity concentration of  $1 \times 10^{17} \text{ cm}^{-3}$  or more can be formed on a semi-insulating GaAs (111) by an epitaxial growth

Art Unit: 1722

method. The silicon thin film layer is formed by a vacuum evaporation method, and an n-type silicon thin film layer (12) is formed by ion implantation of  $P^{+}$ . The ohmic layer (13) is made of platinum (Pt) formed into an insular pattern on the silicon thin film layer (12) by a lift off method. The insular electrode layer (13) is utilized as a mask for plasma etching of the silicon thin film layer (12).

JP '473 A teaches silicon ion implantation into a semi-insulating GaAs substrate (1), comprising a resist layer as a mask and the resist layer has been removed. A SiN film (7) has been removed and a region for the formation of an ohmic electrode has been formed by means of a resist film (8), a Si thin film (3) with a 10 Angstrom thickness, an AuGe film (4) with a 1000 Angstrom thickness, a Ni film (5) with a 300 Angstrom thickness, an Au film with a 1500 Angstrom thickness that can be layered or deposited successively by means of an electron beam in an identical vacuum. After a pattern has been formed by a lift-off method, the means of the resist film (8) is heat-treated, thus becoming an alloy wherein the ohmic electrode is created.

The difference being that JP '460 A does not exactly teach a doped III-V group compound semiconductor single crystal layer, laminating method steps, a metal electrode of aluminum, etc. However, in the absence of unobvious results, it would have been obvious to one of ordinary skill in the art to modify and optimize the semiconductor device, as taught by JP '460 A, with the similar semiconductor device teachings of JP '473 A through routine experimentation in order to ensure proper orientation. The motivation being that an ohmic electrode can be produced with excellent ohmic characteristics.

Art Unit: 1722

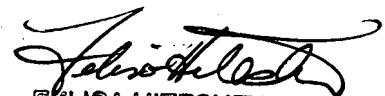
A reference is good not only for what it teaches by direct anticipation but also for what one of ordinary skill might reasonably, infer from the teachings. In re Opprect 12 USPQ 2d 1235, 1236 (CAFC 1989); In re Bode 193 USPQ 12; In re Lamberti 192 USPQ 278; In re Bozek 163 USPQ 545, 549 (CCPA 1969); In re Van Mater 144 USPQ 421; In re Jacoby 135 USPQ 317; In re LeGrice 133 USPQ 365; In re Preda 159 USPQ 342 (CCPA 1968).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Felisa Hiteshew whose telephone number is (571) 272-1463. The examiner can normally be reached on Mondays through Thursday from 5:30 AM to 4:00 PM with Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Yogendra Gupta, can be reached on (571) 272-1316. The

fax phone number for the organization where this application or proceeding is assigned is (571) 273-1463.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866- 217-9197 (toll-free).

  
FELISA HITESHEW  
PRIMARY EXAMINER  
APR 17 2008